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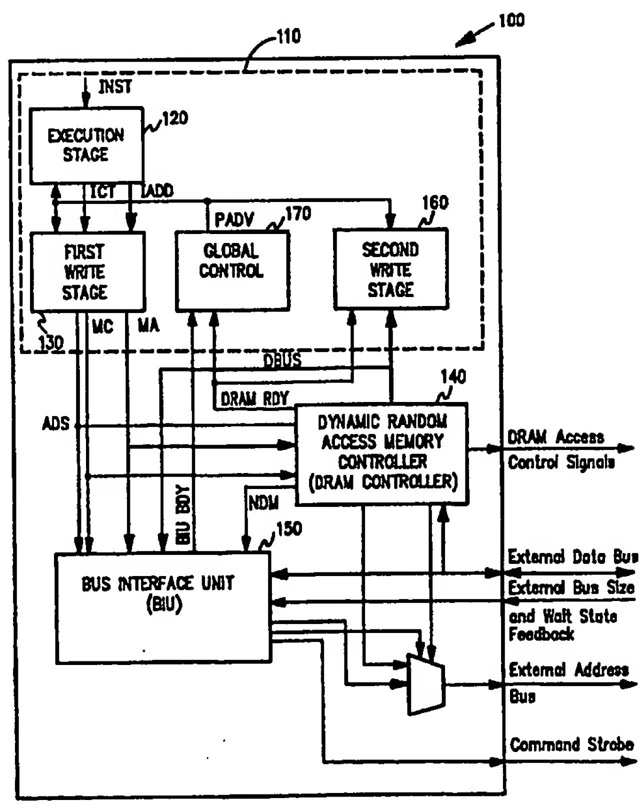
(54) Title: MICROPROCESSOR WITH PIPELINED ACCESS REQUEST TO EXTERNAL MEMORY

(57) Abstract

Memory requests are pipelined to an external memory by forming a memory address during the same clock cycle that the associated instruction is executed, issuing a ready signal during the clock cycle that precedes the clock cycle in which information is output from an external memory, and directing information received from the external memory to a register file during the same clock cycle that the information is received. In addition, when an intruction requires the information that was requested by the previous instruction, the information is directed to an arithmetic logic unit (ALU) during the same clock cycle that the information is received. As a result, the cycle time required to retrieve information stored in a DRAM can be substantially reduced.



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MICROPROCESSOR WITH PIPELINED ACCESS REQUEST TO EXTERNAL MEMORY

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to pipelined microprocessors and, more particularly, to a pipelined microprocessor that pipelines memory requests to an external memory.

2. Description of the Related Art.

A pipelined microprocessor is a microprocessor that operates on instructions in stages so that, at each stage of the pipeline, a different function is performed on an instruction. As a result, multiple instructions move through the pipe at the same time much like to-be-assembled products move through a multistage assembly line.

FIG. 1 shows a block diagram that illustrates the flow of an instruction through a conventional pipelined processor. As shown in FIG. 1, the first stage in the pipe is a prefetch stage. In this stage, the to-be-executed instructions are retrieved from either an instruction cache or an external memory, and are then sequentially loaded into a prefetch buffer. The purpose of the prefetch stage is to fill the prefetch buffer so that one instruction can be advanced to the decode stage, the next stage in the pipe, with each clock cycle.

In the decode stage, each instruction moving through the pipe is decoded to determine what operation is to be performed. After the decode stage, an operand stage determines if data will be needed to perform the operation and, if needed, retrieves the data from memory. Following this, the operation specified by the instruction is performed in an execution stage, while the results of the operation are stored in a write-back stage.

In the ideal case, each instruction is advanced from one stage to the next with each successive clock cycle. Thus, while it takes five clock cycles for an instruction to propagate through the pipeline, the processor appears to complete the execution of each instruction in only one clock cycle.

One situation which can stall the pipeline, or prevent instructions from advancing from one stage to the next with each clock cycle, is the inability of the processor to obtain the data required by the operand stage within a single clock cycle. As a result, conventional pipelined processors typically utilize an on-chip data cache to store the most frequently requested values. Since the data cache is on-chip, the cache can typically be accessed within a single clock cycle.

Although a data cache provides a technique for accessing memory within a single clock cycle, cache memories require a significant amount of silicon real estate to implement, and consume a substantial amount of power each time the cache is accessed. In addition, cache memories further require control logic to insure that each time the data stored in the external memory is updated, the data stored in the cache is also updated.

One solution to these problems is to eliminate the data cache and only utilize the external memory. The primary drawback to this solution, however, is that it takes two to three more clock cycles to retrieve data from the external memory than it does from the cache. Thus, there is a need for a technique that allows the external memory to be accessed within a single clock cycle, thereby eliminating the need for the cache.

SUMMARY OF THE INVENTION

In the present invention, memory requests are pipelined to an external memory by forming a memory address during the same clock cycle that the associated instruction is executed, issuing an early ready signal, and directing the information received from the external memory to a register file during the same clock

cycle that the information is received. In addition, when an instruction requires the information that was requested by a previous instruction, the information received from the external memory can be directed to the arithmetic logic unit (ALU) during the same clock cycle that the information is received. As a result, the cycle time required to retrieve information stored in the external memory can be substantially reduced.

A one-cycle memory access circuit in accordance with the present invention includes a pipelined processor that sequentially advances instructions through the pipe in response to the logic state of a pipeline advance signal. The pipelined processor, in turn, includes an execution stage that latches and executes decoded instructions advanced through the pipe.

When an executed instruction transfers information to or from an external memory, the execution stage forms an internal address that identifies the location in memory where the information is to be transferred to or from during the same clock cycle that the instruction is executed.

The next time the pipeline is advanced, a first write stage of the processor latches the internal address output from the execution stage as a memory address. During the same clock cycle that the memory address is output by the first write stage, a dynamic random-access-memory (DRAM) controller outputs the memory address as a DRAM address when the memory address is within an address space controlled by the DRAM controller.

When information is to be read from memory, the DRAM controller outputs a ready signal during the clock cycle prior to the clock cycle that the information is to be output. The information output onto the data bus is then latched by a second write stage of the processor. The second write stage directs the information to a register file during the same clock cycle that the information is received and, when the information is required by a next instruction, can also direct the information to the ALU in the execution stage.

The advancement of instructions through the pipe is controlled by a global controller that changes the logic state of the pipeline advance signal in response to the logic state of the ready signal when a plurality of pipeline control signals are set to predefined logic states.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings which set forth an illustrative embodiment in which the principals of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the flow of an instruction through a conventional pipelined processor.

FIG. 2 is a block diagram illustrating a one cycle memory access circuit 100 in accordance with the present invention.

FIG. 3 is a timing diagram illustrating the operation of circuit 100 during a series of read operations.

FIG. 4 is a timing diagram illustrating the operation of controller 100 during a series of write operations.

FIG. 5 is a timing diagram illustrating the operation of controller 100 during a combination of read and write operations.

DETAILED DESCRIPTION

FIG. 2 shows a block diagram of a one-cycle memory access circuit 100 in accordance with the present invention. As shown in FIG. 2, circuit 100 includes a pipelined microprocessor 110 that advances instructions through the pipe on the rising edge of a clock signal when a pipeline advance signal PADV, which synchronizes the movement of the instructions, is set to a predefined logic state. Microprocessor 110, in turn, includes an execution stage 120 that latches and executes instructions advanced into the stage.

In accordance with the present invention, when an instruction INST transfers information to or from a DRAM, execution stage 120 also calculates an internal address IADD, which identifies the memory location that corresponds with the instruction, before the next instruction is advanced into the stage.

At the same time, execution stage 120 also sets the logic states of a series of internal control signals ICT that define the memory request associated with the internal address IADD. For example, in the FIG. 2 embodiment, the control signals ICT include a memory/IO signal M/IO# that indicates whether the request is to memory or an I/O device, a data/code signal D/C# that indicates whether the request is for data or code, a byte high enable signal BHE# that indicates which of two bytes of information are to be accessed, a pipe mode signal PipeMd that indicates a pipeline memory access, and a write/read signal W/R# that indicates whether the request is for a read or a write.

As further shown in FIG. 2, microprocessor 110 also includes a first write stage 130 that latches and outputs the internal address IADD as a memory address MA, and the internal control signals ICT as memory control signals MC, when an internal address IADD is advanced into the stage. In addition, first write stage 130 also lowers the logic state of an address strobe ADS, which indicates that the memory address MA is valid, a delay time after a valid internal address is latched.

The memory address MA, the memory control signals MC, and the address strobe ADS are output by first write stage 130 to both a DRAM controller 140 that controls information transfers to and from a series of DRAMs, and a bus interface unit 150 that controls information transfers to and from other external devices.

In response to the memory address MA, the memory control signals MC, and the address strobe ADS, DRAM controller 140 determines whether the memory address MA falls within the address space controlled by controller 140 and, if the address is not within the address space, sets a not DRAM signal NDM to a predetermined logic state. In the FIG. 2 embodiment, BIU controller 150 can not assume control over the external address bus unless the NDM signal is set to the predetermined logic state.

On the other hand, when the memory address MA is within the DRAM address space, and the logic state of the address strobe ADS indicates that the memory address MA is valid, DRAM controller 140 writes information to or reads information from the DRAM identified by the memory address MA. In accordance with the present invention, as described in greater detail below, when information is to be output from the addressed DRAM, controller 140 outputs a ready signal RDY during the clock cycle that precedes the output of the information.

As further shown in FIG. 2, microprocessor 110 also includes a second write stage 160 that latches the information output by the addressed DRAM, and directs the information to a register file. In accordance with the present invention, when the next instruction requires the information output from the addressed DRAM, second write stage 160 also directs the information to the arithmetic logic unit (ALU) in the execution stage during the same clock cycle that the information is received from the addressed DRAM.

For example, if a move instruction, which moves information stored in a DRAM to a first register, is followed by an add instruction, which combines the information stored in the first register with the information stored in a second register, second write stage 160 directs the information from the DRAM to the ALU during the same clock cycle so that the information can be combined with the contents of the second register, thereby saving one clock cycle.

Microprocessor 110 additionally includes a global controller 170 that controls the sequencing of the pipeline. In operation, global controller 170 changes the logic state of the pipeline advance signal PADV each time a plurality of pipeline control signals, including the ready signal RDY, are set to predefined logic states.

FIG. 3 shows a timing diagram that illustrates the operation of controller 100 during a series of read operations. As shown in FIG. 3, a first DRAM read instruction is latched by execution stage 120 on the rising edge of a first processor clock pulse PCLK1 when the pipeline advance signal PADV is asserted. Once

latched, the address ADD1 associated with the first instruction is calculated by execution stage 120 during the first clock period.

Following this, a second DRAM read instruction is latched by execution stage 120 on the rising edge of a second processor clock pulse PCLK2 when the pipeline advance signal PADV is asserted, while address ADD1 is latched as memory address MA1 by first write stage 130. In addition, once the second instruction is latched, the address ADD2 associated with the second instruction is calculated by execution stage 120 during the second clock period.

When memory address MA1 is within the DRAM address space, but is to a different page of memory, DRAM controller 140 drives a row address strobe RAS to a logic high, thereby indicating that the row address is invalid. (Controller 140 also drives the row address strobe high in response to refresh cycle and excessive RAS low indications).

As further shown in FIG. 3, after being driven high, the row address strobe RAS is held high for approximately one and a half processor clock cycles. (The amount of time that the row address strobe RAS must be held high is defined by the DRAM specification).

Once the row address strobe RAS falls, DRAM controller 140 drives a column address strobe CAS to a logic low, which indicates that the column address is valid, approximately one processor clock cycle later. (The amount of time that the column address strobe CAS must be held high following the lowering of the row address strobe RAS is also defined by the DRAM specification). Once the column address strobe CAS is lowered, the information output from the DRAM becomes valid a delay time later.

The ready signal RDY, in turn, indicates to second write stage 160 and global controllr 170 that the information associated with memory address MA1 will be valid during the next clock period.

In addition, global controller 170 sets the logic state of the pipeline advance signal PADV to the predetermined logic state in response to the ready signal RDY, thereby indicating that the instructions in the pipe can be advanced to the next stage in the pipe. As a result, execution stage 120 latches a third instruction on the rising edge of a fourth clock pulse PCLK4, while first write stage 130 latches the second internal address IADD2 as memory address MA2. In addition, second write stage 160 latches the information associated with the first memory address MA1 output from DRAM controller 140 as DRAM information IN1, and directs the information IN1 to one of the register files. As stated above, if the information IN1 is required by the next instruction, second write stage 160 also directs the information IN1 to the ALU.

Thus, in accordance with the present invention, by providing an early ready signal RDY, i.e., by driving the ready signal RDY low, global controller 170 can advance the pipe one cycle early because the information output from the addressed DRAM will be available on the next clock cycle. Therefore, regardless of how many clock cycles are conventionally required to complete a memory request, the present invention allows the request to be completed one clock cycle earlier.

Referring again to FIG. 3, when the second memory address MA2 is to the same page of memory as the first memory address MA1, the column address strobe CAS is dropped again just prior to the falling edge of the fourth processor clock period PCLK4. The information associated with the second memory address MA2 is then latched by second write stage 160 during the fifth clock period as input information IN2.

Thus, in accordance with the present invention, when each memory address relates to the same page of memory as the last memory address, and the row address remains valid, information is read from memory one clock cycle after the address is output. As a result, the present invention allows information to be retrieved from an external memory in the same amount of time that information can be retrieved from a cache memory.

With respect to writing information to an external memory, the present invention allows information to be written during the same clock cycle that the associated memory address is output by first write stage 130 when the address relates to the same page of memory, and the row address remains valid.

FIG. 4 shows a timing diagram that illustrates the operation of controller 100 during a series of write operations. As shown in FIG. 4, information is written to a DRAM in the same way that information is read from a DRAM except that the information is latched by the DRAM when the column address strobe CAS is lowered.

FIG. 5 shows a timing diagram that illustrates the operation of controller 100 during a combination of read and write operations. As shown in FIG. 5, read and write requests can occur at a rate of one request per cycle. In addition, a one cycle gap is required between read and write requests to avoid a collision on the data bus.

In accordance with the present invention, in addition to pipelining memory requests output from execution stage 120, circuit 100 can also pipeline memory requests from a prefetch stage. When memory requests are pipelined from the prefetch stage, first write stage 130 includes a multiplexer that passes either the address and control signals output from the execution stage, or the address and control signals output from the prefetch stage.

As stated above, in addition to the ready signal RDY, a plurality of pipeline control signals are utilized by global controller 170 to determine when the instructions in the pipe are to be advanced. The pipeline control signals, in turn, include double word and misaligned byte signals.

In the FIG. 2 embodiment, two bytes of information are associated with each memory address. Thus, a double word signal indicates that the information associated with two successive memory locations is requested. On the other hand, the misaligned byte signal indicates when the word of information includes one byte from one address and one byte from another address.

When the execution stage or the prefetch stage output a double word or a misaligned byte signal, global controller 170 ignores the first ready signal, and advances the pipe in response to the second ready signal.

The invention embodiments described herein have been implemented in an integrated circuit which includes a number of additional functions and features which are described in the following co-pending, commonly assigned patent applications, the disclosure of each of which is incorporated herein by reference: U.S. patent application Serial No. 08/__________, entitled "DISPLAY CONTROLLER CAPABLE OF ACCESSING AN EXTERNAL MEMORY FOR GRAY SCALE MODULATION DATA" (atty. docket no. NSC1-62700); U.S. patent application Serial No. 08/__________, entitled "SERIAL INTERFACE CAPABLE OF OPERATING IN TWO DIFFERENT SERIAL DATA TRANSFER MODES" (atty. docket no. NSC1-62800); U.S. patent application Serial No. 08/__________, entitled "HIGH PERFORMANCE MULTIFUNCTION DIRECT MEMORY ACCESS (DMA) CONTROLLER" (atty. docket no. NSC1-62900); U.S. patent application Serial No. 08/__________, entitled "OPEN DRAIN MULTI-SOURCE CLOCK GENERATOR HAVING MINIMUM PULSE WIDTH" (atty. docket no. NSC1-63000); U.S. patent application Serial No. 08/__________, entitled "INTEGRATED CIRCUIT WITH MULTIPLE FUNCTIONS SHARING MULTIPLE INTERNAL SIGNAL BUSES ACCORDING TO DISTRIBUTED BUS ACCESS AND CONTROL ARBITRATION" (atty. docket no. NSC1-63100); U.S. patent application Serial No. 08/__________, entitled "EXECUTION UNIT ARCHITECTURE TO SUPPORT x86 INSTRUCTION SET AND x86 SEGMENTED ADDRESSING" (atty. docket no. NSC1-63300); U.S. patent application Serial No. 08/__________, entitled "BARREL SHIFTER" (atty. docket no. NSC1-63400); U.S. patent application Serial No. 08/__________, entitled "BIT SEARCHING THROUGH 8, 16, OR 32-BIT OPERANDS USING A 32-BIT DATA PATH" (atty. docket no. NSC1-63500); U.S. patent application Serial No. 08/__________, entitled "DOUBLE PRECISION (64-BIT) SHIFT OPERATIONS USING A 32-BIT DATA PATH" (atty. docket no. NSC1-63600); U.S. patent application Serial No. 08/__________, entitled "METHOD FOR PERFORMING SIGNED DIVISION" (atty. docket no. NSC1-63700); U.S. patent application Serial No. 08/__________, entitled "METHOD FOR PERFORMING ROTATE THROUGH CARRY USING A 32-BIT BARREL SHIFTER AND COUNTER" (atty. docket no. NSC1-63800); U.S. patent application Serial No. 08/__________, entitled "AREA AND TIME EFFICIENT

FIELD EXTRACTION CIRCUIT" (atty. docket no. NSC1-63900); U.S. patent application Serial No. 08/_________, entitled "NON-ARITHMETICAL CIRCULAR BUFFER CELL AVAILABILITY STATUS INDICATOR CIRCUIT" (atty. docket no. NSC1-64000); U.S. patent application Serial No. 08/_________, entitled "TAGGED PREFETCH AND INSTRUCTION DECODER FOR VARIABLE LENGTH INSTRUCTION SET AND METHOD OF OPERATION" (atty. docket no. NSC1-64100); U.S. patent application Serial No. 08/_________, entitled "PARTITIONED DECODER CIRCUIT FOR LOW POWER OPERATION" (atty. docket no. NSC1-64200); U.S. patent application Serial No. 08/_________, entitled "CIRCUIT FOR DESIGNATING INSTRUCTION POINTERS FOR USE BY A PROCESSOR DECODER" (atty. docket no. NSC1-64300); U.S. patent application Serial No. 08/_________, entitled "CIRCUIT FOR GENERATING A DEMAND-BASED GATED CLOCK" (atty. docket no. NSC1-64500); U.S. patent application Serial No. 08/_________, entitled "INCREMENTOR/DECREMENTOR" (atty. docket no. NSC1-64700); U.S. patent application Serial No. 08/_________, entitled "A PIPELINED MICROPROCESSOR THAT PIPELINES MEMORY REQUESTS TO AN EXTERNAL MEMORY" (atty. docket no. NSC1-64800); U.S. patent application Serial No. 08/_________, entitled "CODE BREAKPOINT DECODER" (atty. docket no. NSC1-64900); U.S. patent application Serial No. 08/_________, entitled "TWO TIER PREFETCH BUFFER STRUCTURE AND METHOD WITH BYPASS" (atty. docket no. NSC1-65000); U.S. patent application Serial No. 08/_________, entitled "INSTRUCTION LIMIT CHECK FOR MICROPROCESSOR" (atty. docket no. NSC1-65100); U.S. patent application Serial No. 08/_________, entitled "A PIPELINED MICROPROCESSOR THAT MAKES MEMORY REQUESTS TO A CACHE MEMORY AND AN EXTERNAL MEMORY CONTROLLER DURING THE SAME CLOCK CYCLE" (atty. docket no. NSC1-65200); U.S. patent application Serial No. 08/_________, entitled "APPARATUS AND METHOD FOR EFFICIENT COMPUTATION OF A 486™ MICROPROCESSOR COMPATIBLE POP INSTRUCTION" (atty. docket no. NSC1-65700); U.S. patent application Serial No. 08/_________, entitled "APPARATUS AND METHOD FOR EFFICIENTLY DETERMINING ADDRESSES FOR MISALIGNED DATA STORED IN MEMORY" (atty. docket no. NSC1-65800); U.S. patent application Serial No. 08/_________, entitled "METHOD OF IMPLEMENTING FAST 486™ MICROPROCESSOR COMPATIBLE STRING OPERATION" (atty. docket no. NSC1-65900); U.S. patent application Serial No. 08/_________, entitled "A PIPELINED MICROPROCESSOR THAT PREVENTS THE CACHE FROM BEING READ WHEN THE CONTENTS OF THE CACHE ARE INVALID" (atty. docket no. NSC1-66000); U.S. patent application Serial No. 08/_________, entitled "DRAM CONTROLLER THAT REDUCES THE TIME REQUIRED TO PROCESS MEMORY REQUESTS" (atty. docket no. NSC1-66300); U.S. patent application Serial No. 08/_________, entitled "INTEGRATED PRIMARY BUS AND SECONDARY BUS CONTROLLER WITH REDUCED PIN COUNT" (atty. docket no. NSC1-66400); U.S. patent application Serial No. 08/_________, entitled "SUPPLY AND INTERFACE CONFIGURABLE INPUT/OUTPUT BUFFER" (atty. docket no. NSC1-66500); U.S. patent application Serial No. 08/_________, entitled "CLOCK GENERATION CIRCUIT FOR A DISPLAY CONTROLLER HAVING A FINE TUNEABLE FRAME RATE" (atty. docket no. NSC1-66600); U.S. patent application Serial No. 08/_________, entitled "CONFIGURABLE POWER MANAGEMENT SCHEME" (atty. docket no. NSC1-66700); U.S. patent application Serial No. 08/_________, entitled "BIDIRECTIONAL PARALLEL SIGNAL INTERFACE" (atty. docket no. NSC1-67000); U.S. patent application Serial No. 08/_________, entitled "LIQUID CRYSTAL DISPLAY (LCD) PROTECTION CIRCUIT" (atty. docket no. NSC1-67100); U.S. patent application Serial No. 08/_________, entitled "IN-CIRCUIT EMULATOR STATUS INDICATOR CIRCUIT" (atty. docket no. NSC1-67400); U.S. patent application Serial No. 08/_________, entitled "DISPLAY CONTROLLER CAPABLE OF ACCESSING GRAPHICS DATA FROM A SHARED SYSTEM MEMORY" (atty. docket no. NSC1-67500); U.S. patent application Serial No. 08/_________, entitled "INTEGRATED CIRCUIT WITH TEST SIGNAL BUSES AND TEST CONTROL CIRCUITS" (atty. docket

no. NSC1–67600); U.S. patent application Serial no. 08/__________, entitled "DECODE BLOCK TEST METHOD AND APPARATUS" (atty. docket no. NSC1–68000).

It should be understood that various alternatives to the embodiment of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that methods and structures within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A one-cycle memory access circuit for pipelining memory requests to an external memory, the circuit comprising:

a pipelined processor having

an execution stage that forms and outputs an internal address in response to an instruction that transfers information to or receives information from an external memory when a pipeline advance signal is set to a predefined logic state and a first plurality of control signals are set to predefined logic states at a point during a first clock period,

a first write stage that latches and outputs the internal address output from the execution stage as a memory address when the pipeline advance signal is set to the predefined logic state at a point during a second clock period,

a second write stage that latches and inputs information from a data bus during a third clock cycle when a ready signal is set to a predefined logic state during the second clock period, and

a global controller that changes the logic state of the pipeline advance signal in response to the logic state of the ready signal when a second plurality of control signals are set to predefined logic states; and

a dynamic random-access-memory (DRAM) controller that requests information associated with the memory address from a DRAM during the second clock period when the memory address is within an address space controlled by the DRAM controller, the memory address is to a same page of memory as a last memory address, and a row address strobe indicates that the row address of the last memory address remains valid, that captures the information associated with the memory address output by the DRAM during the second clock period, and that outputs the information onto the data bus during the third clock period.

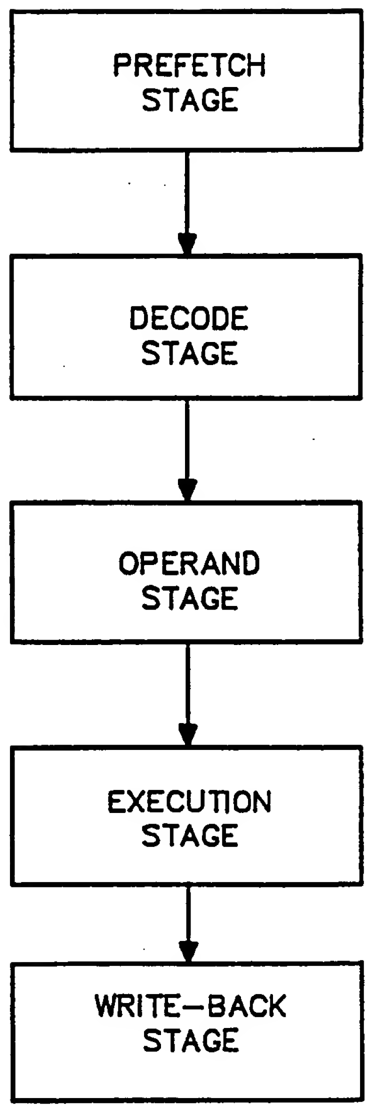
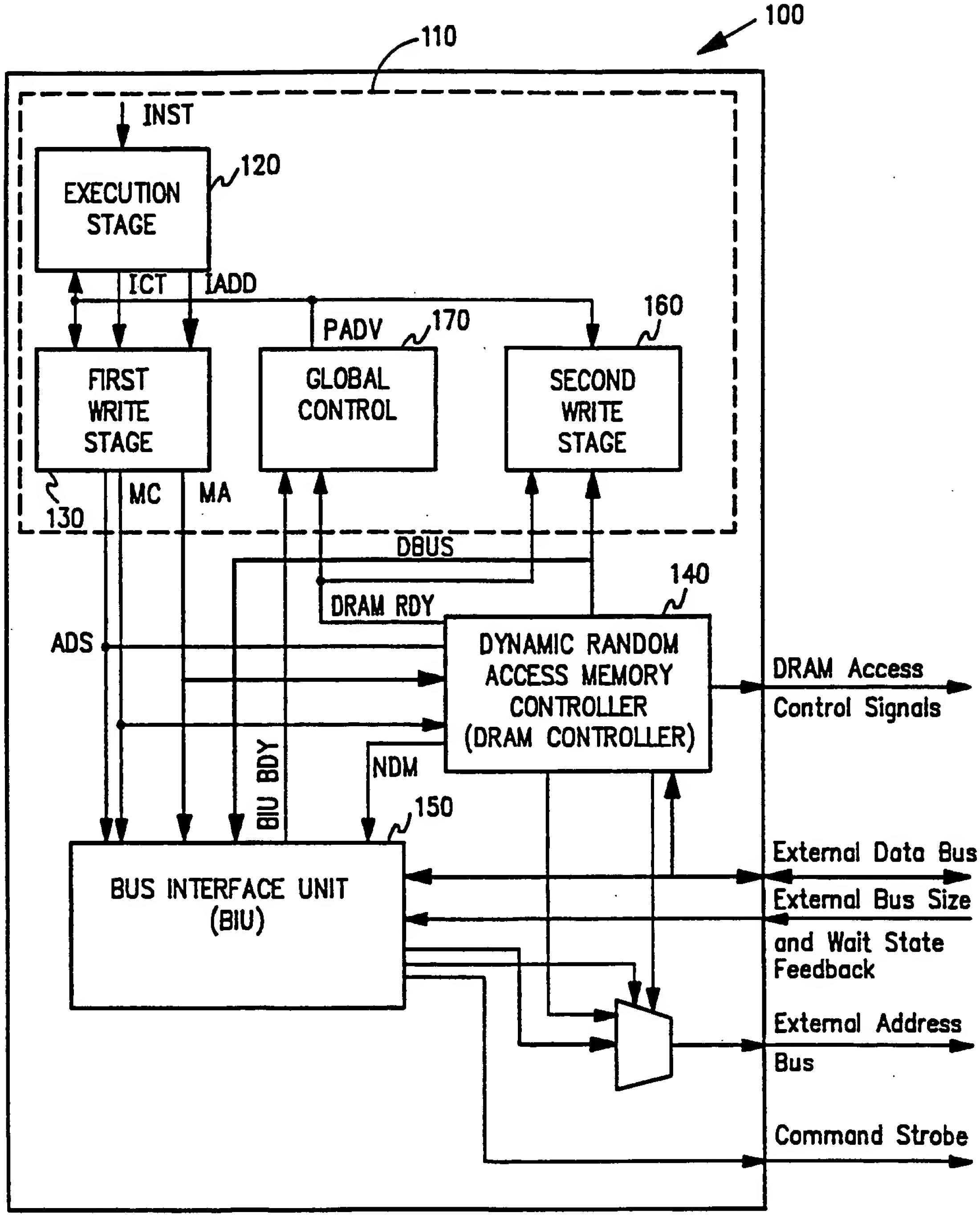


FIG. 1
PRIOR ART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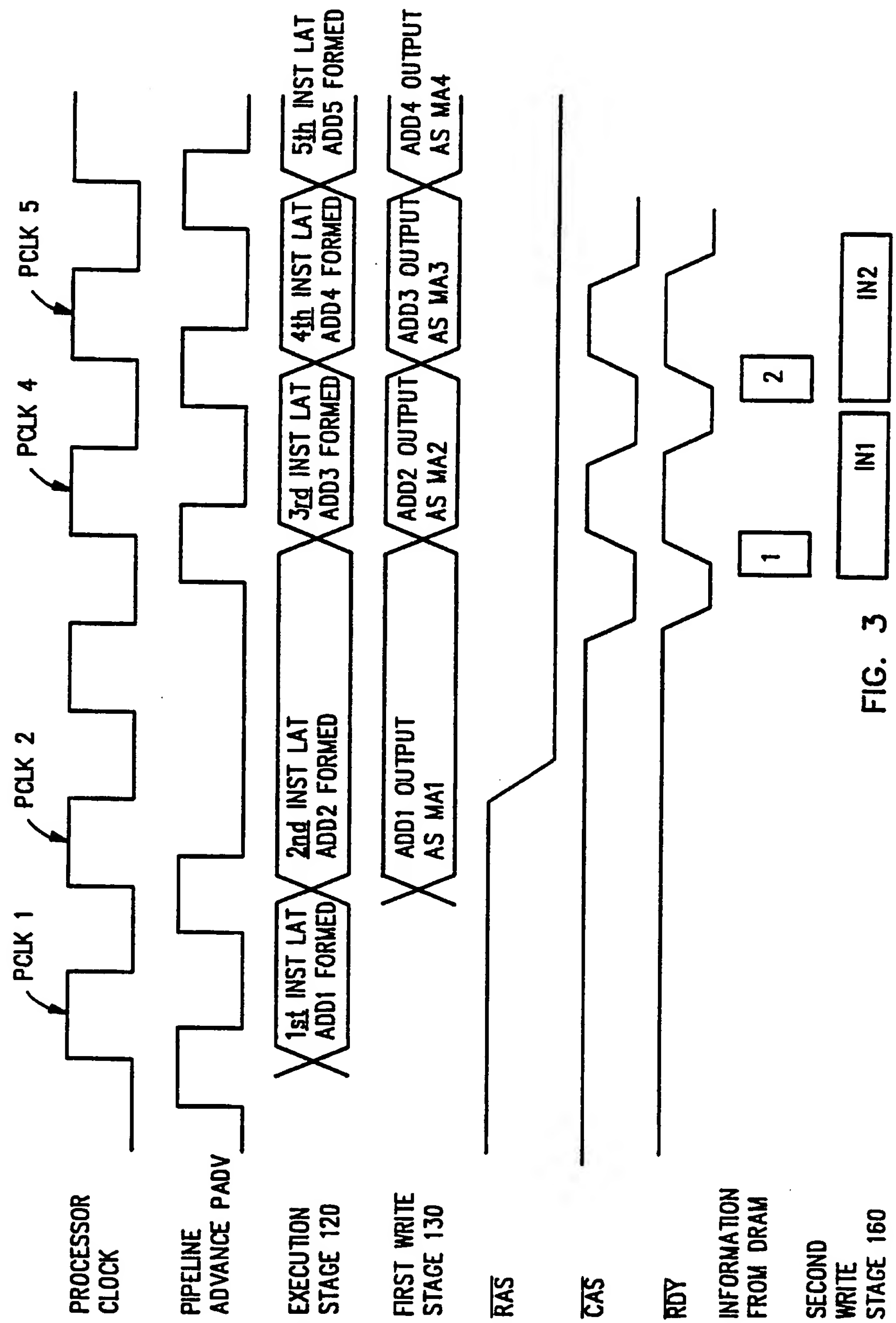
External Bus Size and Wait State Feedback
External Address Bus
Command Strobe

FIG. 2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PCLK 2
PCLK 4
PCLK 5
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3rd INST LAT ADD3 FORMED
4th INST LAT ADD4 FORMED
5th INST LAT ADD5 FORMED
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ADD2 OUTPUT AS MA2
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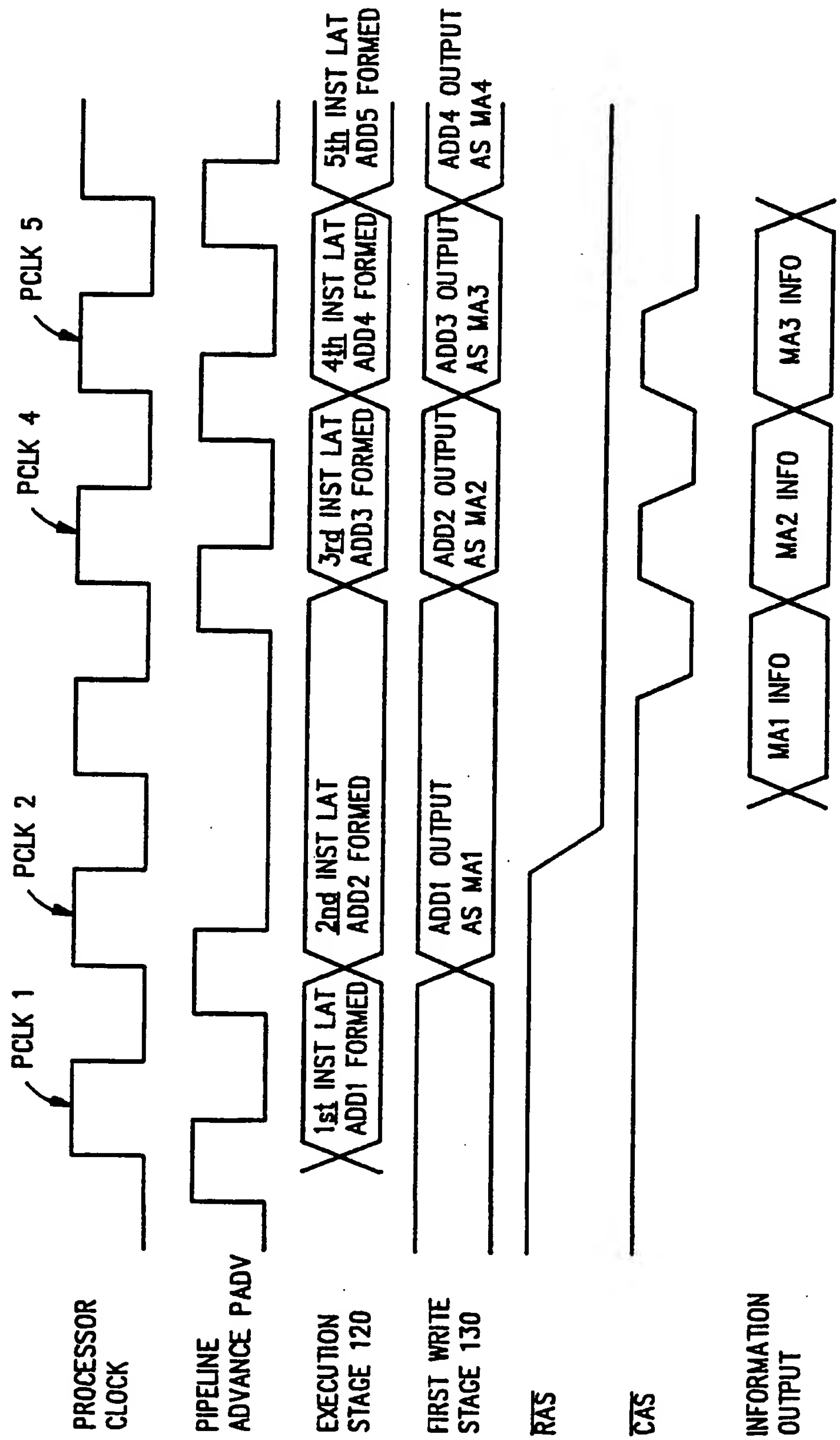
ADD4 OUTPUT AS MA4
1
2
IN1
IN2

FIG. 3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MA1 INFO
MA2 INFO
MA3 INFO

FIG. 4

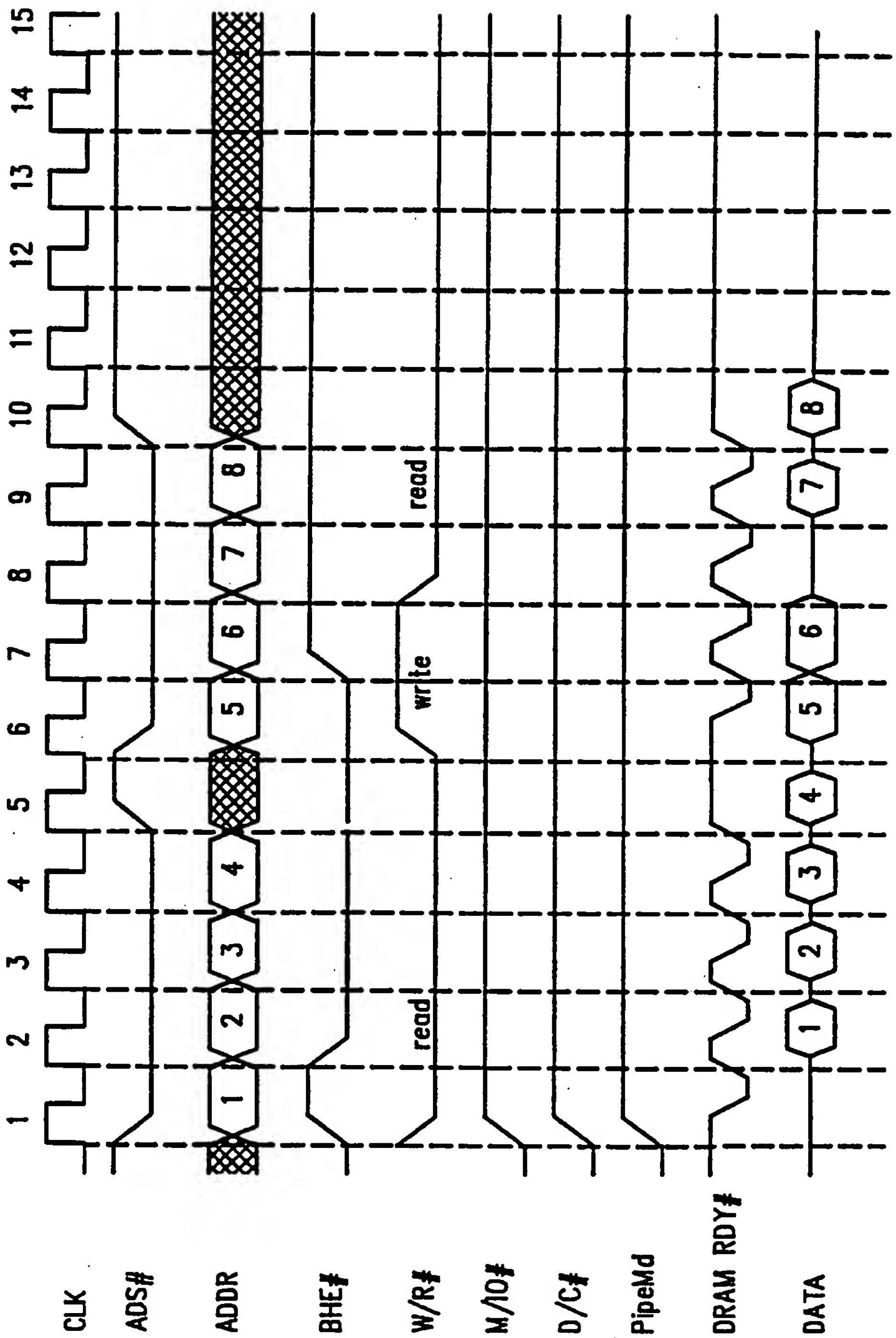
CLK
ADS#
ADDR
BHE#
W/R#
M/IO#
D/C#
PipeMd
DRAM RDY#
DATA
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
read
write
read

FIG. 5

INTERNATIONAL SEARCH REPORT

Inte   'ional Application No
PCT/US 96/07586

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 398 382 (TOKYO SHIBAURA ELECTRIC CO) 22 November 1990 see the whole document ---	1
A	US,A,5 239 639 (FISCHER STEPHEN A ET AL) 24 August 1993 see the whole document ---	1
A	JOURNAL OF SUPERCOMPUTING, vol. 7, no. 1/02, 1 May 1993, pages 143-180, XP000422830 BECK G R ET AL: "THE CYDRA 5 MINISUPERCOMPUTER: ARCHITECTURE AND IMPLEMENTATION" see page 172, paragraph 4 ---	1
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

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Date of the actual completion of the international search	Date of mailing of the international search report
10 October 1996	15. 10. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Daskalakis, T

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INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 96/07586

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 25, no. 1, 1 February 1990, NEW YORK US, pages 100-106, XP000101855 KAZUTAKA NOGAMI ET AL: "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC" * page 101, section IV: "Pipelined Operation" * ---	1
A	IEEE MICRO, vol. 15, no. 2, 1 April 1995, pages 33-43, XP000499003 EDMONDSON J H ET AL: "SUPERSCALAR INSTRUCTION EXECUTION IN THE 21164 ALPHA MICROPROCESSOR" -----	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr nal Application No
PCT/US 96/07586

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		JP-B-	7007356	30-01-95
		US-A-	5197134	23-03-93
		US-A-	5228370	20-07-93
US-A-5239639	24-08-93	JP-A-	6028238	04-02-94